A STUDY OF QUANTIZATION NOISE EFFECT IN A DELTA-SIGMA ANALOG TO DIGITAL CONVERTER

Alban RAKIPI, Aleksandër BIBERAJ, Indrit ENESI
Faculty of Information Technology, Polytechnic University of Tirana, Albania

ABSTRACT

Digital technology increasingly pervades daily life, and the use of innovative techniques in analog-to-digital converter (ADC) schemes has become particularly important. Nowadays, analog to digital converters are crucial components in almost any electronic systems. Some of the most important aspects are related to the development and implementation of schemes that are energy efficient, that offer very high conversion accuracy, that suppress distortions, and are more immune to various noise sources. A problem that is widely encountered in ADC converters is quantization noise, which affects resolution, the correspondence between samples, induced delays, and limitations in developing higher order circuits. The quantization noise effect of a delta-sigma analog to digital converter is in the present paper investigated. Randomly generated quantization noise samples are used to evaluate the output performance of the converter, by measuring the signal to noise (SNR) ratio. In the simulated scenario are considered the following parameters: filter length, oversampling ratio, transition bandwidth and decimation factor. Optimal values of these parameters are suggested in order to reduce the noise effect and to improve SNR.

***Keywords*:** Analog-to-digital converter, delta-sigma, noise, quantization

1. INTRODUCTION

A delta-sigma ADC is used in various conversion systems to obtain a low-power, high-accuracy conversion using oversampling and noise shaping for audio, sensor, and wireless applications (Saikatsu and Yasuda, 2019). Successive approximation register (SAR) and delta-sigma (ΔΣ) architectures using oversampling techniques have recently gained popularity of ADC with high energy efficiency in the bandwidth range under tens of mega-hertz (Fukazawa *et al*., 2020).

In many modern electronic systems, analog to digital converters are essential components because they are responsible for converting a measured analog signal into a digital representation. The conversion of an analog signal to a digital one frequently restricts the overall system's speed and resolution. As a result, A/D converters that accomplish both high speed and resolution are required. Many image, communication, and instrumentation systems could benefit from such converters (Katara *et al*., 2012).

Pipeline, SAR, and delta- sigma modulators currently dominate the state of the art in analog-to-digital converters, which continue to push the boundaries of energy efficiency year after year (de La Rosa *et al*., 2015). The signal-to-noise ratio (SNR), measured in decibels, is a critical performance metric for different applications. Many external noise sources, such as clock noise, power supply noise, might affect the ADCs utilized in these systems (Reeder *et al*., 2005).

Fukazawa *et al.*, (2020) showed a quantization error extraction method that considers the quantizer delay and prevents the input leakage to the second stage to suppress distortion. The addition of a digital integrator reduces the amplitude of the quantizer input, preventing quantizer saturation.

Bajaj *et al*., (2020) presented a 12-bit successive approximation analog-to-digital converter embedded in a first-order noise shaping loop to obtain a 16-bit resolution while maintaining sample-by-sample correspondence. The need for high oversampling in ΔΣ A/D converters has limited their use to primarily low frequency applications (Katara *et al*., 2012).

A new method for extracting the VCO quantization noise is proposed in (Maghami *et al*., 2019). Using the proposed technique, in the time domain, the quantization noise of a VCO-based quantizer is extracted precisely as a PWM signal. By applying this pulse signal to another VCO-based quantizer, higher order structures could be implemented.

Increasing the gain coefficient of the integrator in the loop filter configuration of the delta-sigma ADC suppresses the quantization noise that occurs in the signal band. However, there is a trade-off relationship between the integrator gain coefficient and system stability (Saikatsu and Yasuda, 2019). Saikatsu and Yasuda (2019) proposed a SC integrator with the structure of a finite impulse response (FIR) filter in a loop filter configuration. This structure can realize broadband and high-precision performance, a high signal-to-quantization noise ratio, and increased integrator gain in the signal band.

The present paper evaluates the quantization noise effect of a ΔΣ A/D converter, by taking into consideration the length of the FIR filter, the oversampling ratio, the transition bandwidth and the decimation factor. The simulated results are compared with the theorical ones. The rest of the paper is outlined as follows. Section 2 describes the main architecture of a ΔΣ A/D

converter. Section 3 informs about simulation scenarios and reports the results. Section 4 makes conclusions.

2. THE DELTA – SIGMA ADC ARCHITECTURE

Delta-sigma (ΔΣ) ADCs with oversampling and noise-shaping are the most utilized ADCs for achieving high resolution among all categories (Tan *et al.*, 2020). Due to the requirement for high oversampling in A/D converters, their usage has been limited to mainly low frequency applications (Katara *et al.*, 2012).

Oversampling ADCs with a feedback loop have been created to further minimize noise in the low-frequency region; the most prevalent today is the A/D converter. The architecture of a such converter is in Figure 1 depicted. The serial bit stream coming out of the comparator contains the average value of the input voltage (1-bit ADC). The serial bit stream is processed by the digital filter and decimator, which produces the final output data (Kester 2009b).

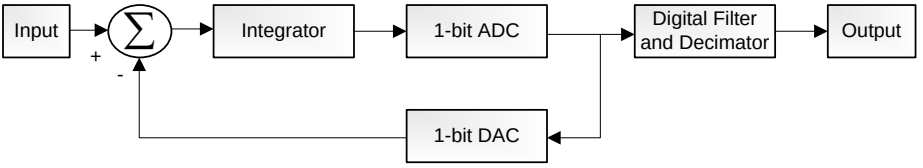


Fig. 1. The architecture of a first order delta-sigma ADC.

Given a signal power $E\left\{\left|x\right|^2\right\}$ and a noise power $E\left\{\left|n_q\right|^2\right\}=\sigma_q^2$ the output SNR is given by equation in (1) (Martin 2012):

$$\left(\frac{S}{N}\right)_{out}=\frac{E\left\{\left|y_x\right|^2\right\}}{E\left\{\left|y_n\right|^2\right\}}=\frac{E\left\{\left|x\right|^2\right\}}{2\sigma_q^2} \qquad (1)$$

However, it should be considered that the signal $x(t)$ can be highly oversampled, and low-pass filtering can reduce the final quantization noise.

Given an over-sampling ratio (OSR) in equation (2) (Martin 2012)

$$OSR=K=\frac{f_s}{2B_x} \qquad (2)$$

the actual noise power after decimation and down-sampling can be evaluated from the scheme in Figure 2 (Kester 2009a).

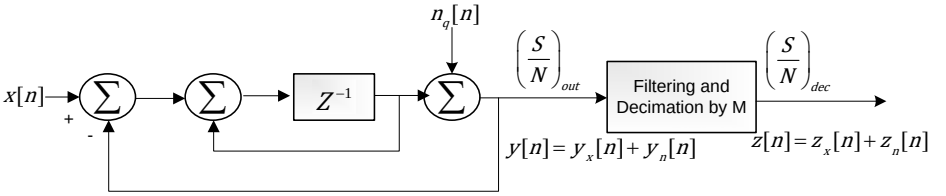


Fig. 2. The block-diagram for SNR evaluation after filtering and decimation.

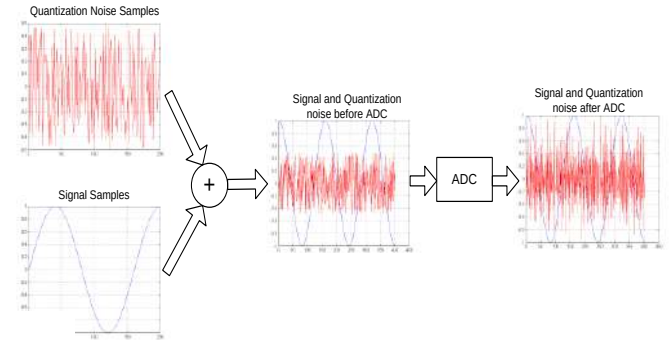
Once sampling occurs, filtering and decimation are carried out by the actual ADC to eliminate the quantization noise. For K much greater than one the signal to noise ratio after decimation is given by the formula in (3) as reported in (Martin 2012):

$$\left(\frac{S}{N}\right)_{dec} = \frac{E\left\{\left|Z_x\right|^2\right\}}{E\left\{\left|Z_n\right|^2\right\}} = \frac{E\left\{\left|x\right|^2\right\}}{2\sigma_q^2\left[\frac{1}{K} - \frac{1}{\pi}\sin\left(\pi\frac{1}{K}\right)\right]} = 3K^3\frac{E\left\{\left|x\right|^2\right\}}{2\sigma_q^2\pi^2} \qquad (2)$$

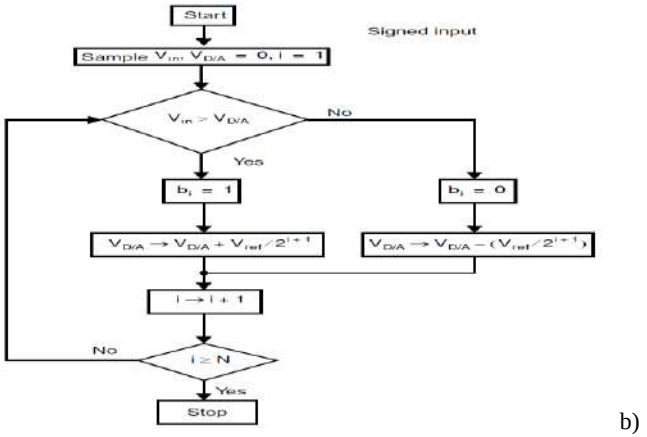
If good decimation filters can be designed, the SNR performance of Δ-Σ ADC improves with the oversampling ratio K.

3. SIMULATION SCENARIO AND RESULTS

The simulation of the delta-sigma ADC is modeled using MATLAB. The conceptual block-diagram of the simulation scenario is given in Fig. 3a. Randomly generated quantization noise samples (white noise) are added to the pure sinewave signal to be converted. The conversion algorithm used is based on the binary search algorithm which determines the closest digital word to match an input signal (Martin 2012). The flow-chart using a successive-approximation approach is shown in Figure 3b.



a)



b)

Fig. 3: a) Conceptual block-scheme for quantization noise evaluation, b) Flow chart for the successive-approximation algorithm (Martin 2012).

In our scenario four different parameters are considered. In the first run, the filter length parameter, LFIR is changed from 500 (the default value) to 400 and 600 with respect to the same oversampling ratio K, and the results are in Figure 4 and 5 depicted.

The Figure 4 and 5 show that as number of the filter coefficients (filter length LFIR) increases, a better SNR performance could be achieved. The initial SNR value is a little bit higher in a case of LFIR = 600 than in the case of LFIR = 400 and obtained SNR curve (the blue curve) almost follows the trend as the theoretical one (the red curve). With the lower filter length (400) the SNR values linearly decrease with the gradient proportional to a drop in LFIR.

In the second run, the oversampling factor K is considered to see whether the SNR performance can be improved. In the MATLAB routine the K value

is changed. A comparison for the chosen values of K = 80 and K = 140, are in Figure 6 and 7 depicted.

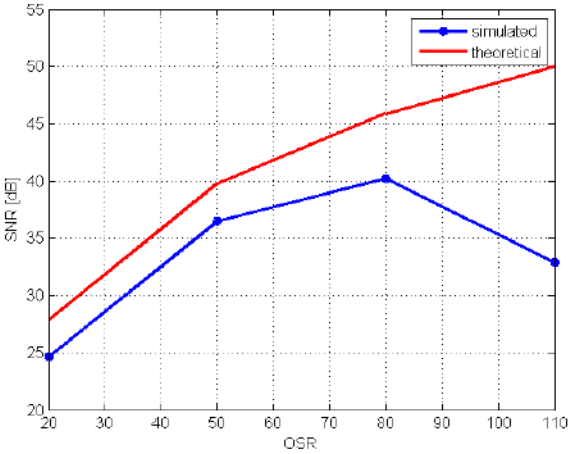


Fig. 4: SNR after filtering in Delta-Sigma ADC for LFIR=400.

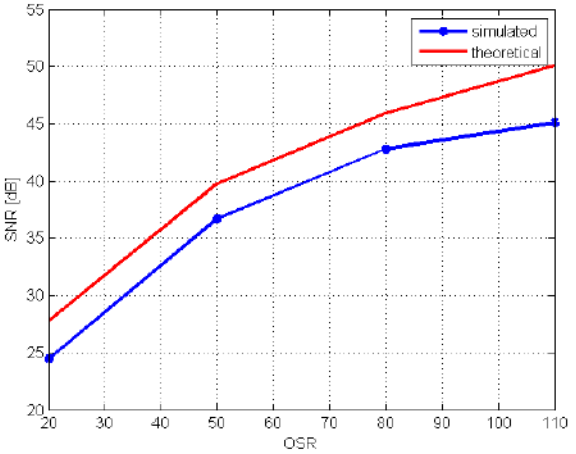


Fig. 5: SNR after filtering in Delta-Sigma ADC for LFIR=600.

The results show that SNR performance significantly change with the change of an oversampling ratio K. The SNR curve becomes almost linear as K decreases. In addition, it behaves as the theoretical with the lower SNR values. It is known that the signal can be highly oversampled and low-pass filtering can reduce the final quantization noise. With down-conversion of a

digital signal the oversampling factor decreases (K↓). Figure 6 and 7 show that for the lower K values (20-40) the SNR performance improves. A drop in SNR performance follows the rest of the graph.

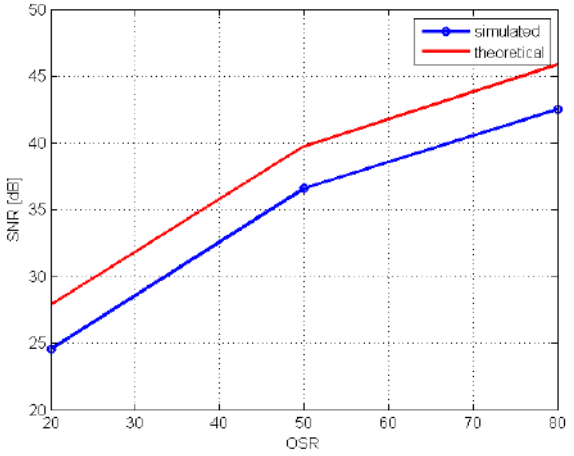


Fig. 6: SNR after filtering in Delta-Sigma ADC for K = 80.

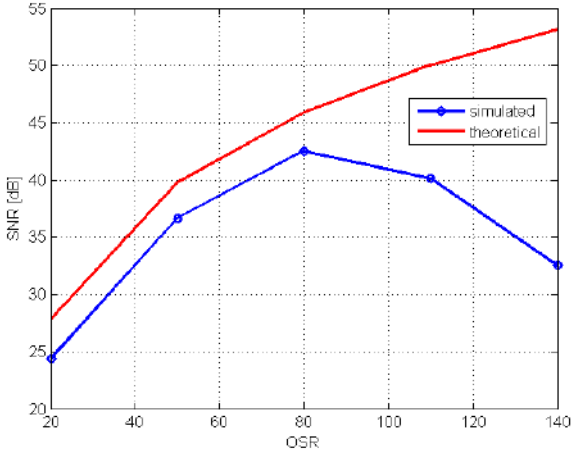


Fig. 7. SNR after filtering in Delta-Sigma ADC for K = 140.

In the third run, the impact of transition bandwidth in SNR is investigated. The performance is evaluated depending on the changes of the $band_1$ and $band_2$. $Band_1$ presents the filter passband and $band_2$ a lower limit of the filter stop-band. The filter transition band is the difference between $band_2$ and $band_1$. Both bands depend on the signal bandwidth f_0. The latter depends on

the normalized sampling frequency f_S and an oversampling factor K. The results are in Figure 8 and 9 shown.

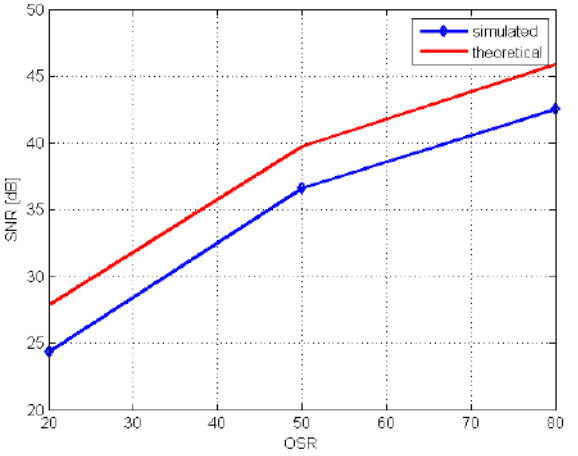


Fig. 8: SNR after filtering in Delta-Sigma ADC for the transition bandwidth where ($band_2=2.2f_0$ and $band_1=1.2f_0$)

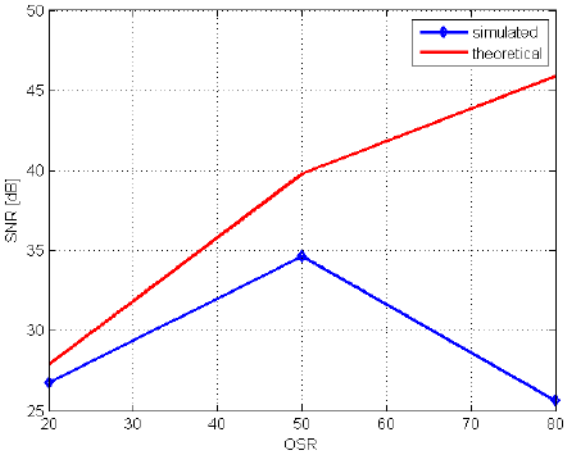


Fig. 9: SNR after filtering in Delta-Sigma ADC for the smaller transition bandwidth ($band_2=1.6f_0$ and $band_1=1.2f_0$).

Results show that the SNR performance drops as the difference between the filter passband and the lower limit of the filter stop-band becomes smaller. So, the smaller the transition bandwidth is, the lower the SNR values are (Figure 8). If the transition bandwidth is narrowed, the attenuation increases. Consequently, transition bandwidth is the critical parameter, not the

bandwidth. The SNR performance improves as increase the transition bandwidth increases. We changed the multiple rates of the signal bandwidth to get different values of $band_1$ and $band_2$, and therefore a larger value of the filter transition bandwidth. With a wider transition bandwidth, the measured SNR performance after filtering closely follows the theoretical one (Figure 11).

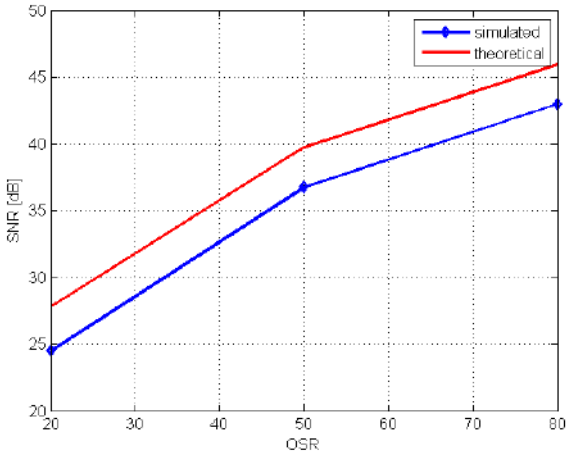


Fig. 10: SNR after filtering in Delta-Sigma ADC for the transition bandwidth ($band_2=2.4f_0$ and $band_1=1.0f_0$).

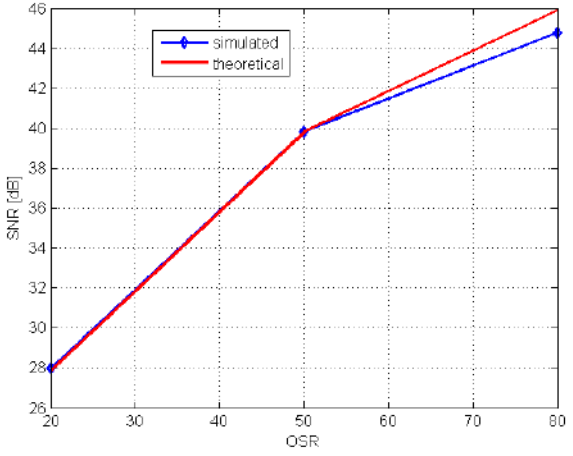


Fig. 11: SNR after filtering in Delta-Sigma ADC for the transition bandwidth ($band_2=1.8f_0$ and $band_1=0.8f_0$)

In the last run, the SNR behavior with respect to a decimation factor L is evaluated. When a digital signal is up converted, a decimation is performed by generating its replicas. With the decimation factor equal to 10, is obtained the SNR plot of Figure 12. Here we cold note that the initial SNR value is a little bit lower due to a lower limit of the filter stop-band inversely proportional to the decimation factor L. In the next step we modified L value to L = 6, L = 7 and L = 8, and the results are shown in Figures 13-15.

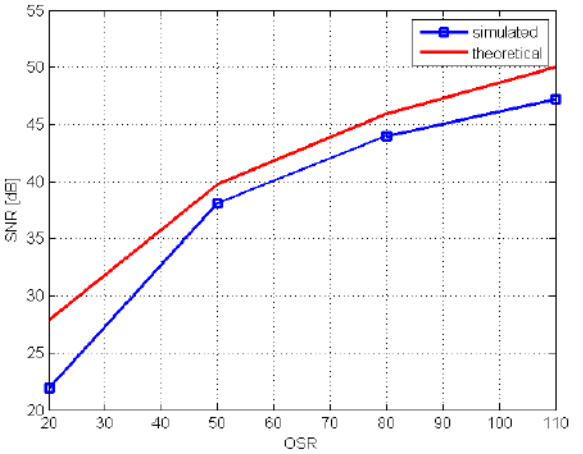


Fig. 12: SNR after filtering in Delta-Sigma ADC for L = 10.

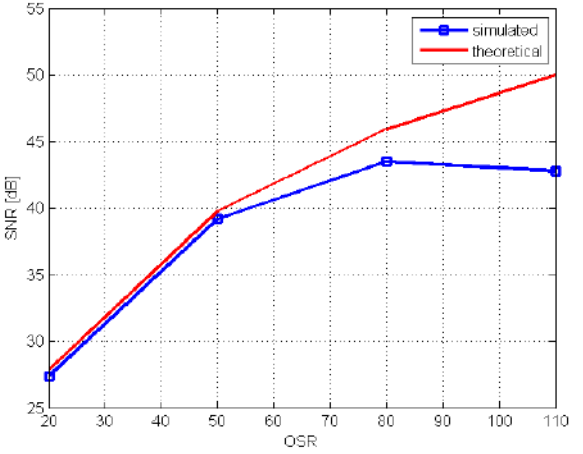


Fig. 13: SNR after filtering in Delta-Sigma ADC for L = 6.

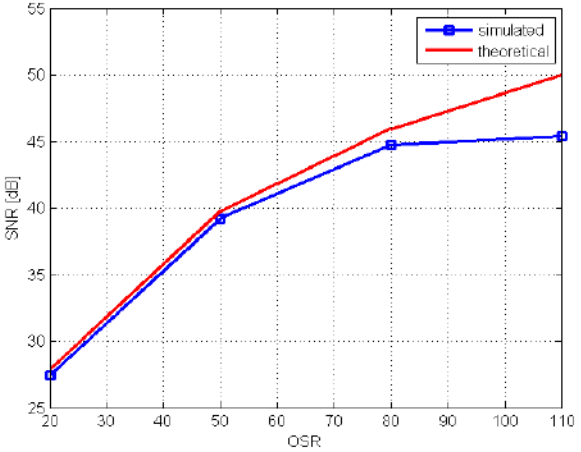


Fig. 14: SNR after filtering in Delta-Sigma ADC for L = 7.

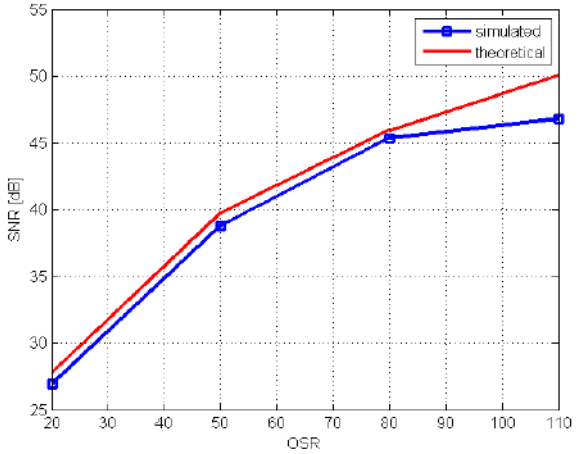


Fig. 15: SNR after filtering in Delta-Sigma ADC for L = 8.

Based on figures, it could be concluded that as the decimation factor increases, the initial SNR values get lower with respect to the theoretical ones. In the first step (K from 20 to 50) the measured SNR curve is becoming closer to the theoretical. In the second step (K from 50 to 80) they are increasing by the same gradient, and in the third step (K from 80 to 110) the measured diverges from the theoretical with a different increasing slope. By setting a lower decimation factor (L = 8) both SNR curves are approximately the same up to oversampling factor K = 80.

4. CONCLUSIONS

In present paper investigates the quantization noise effect and SNR performance of a delta-sigma ADC. The results show that the higher the number of the filter coefficients (filter length LFIR) is, the better SNR values with the higher oversampling factor K are.

The oversampling factor K should be high enough to ensure better SNR values after filtering in Delta-Sigma ADC, but with some limited value since with some high values of K the measured SNR performance deviate from the theoretical one.

The transition bandwidth, as a difference of passband and a lower limit of the stopband, should be larger and chosen in such a manner that SNR curve reaches optimal values; both bandwidths depend on the f_S and f_0 and should be chosen in an optimal proportion. If the transition bandwidth is increased, the attenuation increases. Consequently, the transition bandwidth is the critical parameter, not the bandwidth.

Both filtering and decimation could be carried out at a lower speed, and by properly choosing decimation factor it is possible to reduce the noise effect and consequently improve SNR.

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